REMARKS

The January 5, 2006 Office Action was based upon pending Claims 1-12. The Examiner rejected Claims 1-12. This Amendment amends Claims 1, 6, 7 and 11 and cancels Claims 3 and 8. Thus, after entry of this Amendment, Claims 1, 2, 4-7 and 9-12 are pending and presented for further consideration. The foregoing amendments and the following comments are responsive to the rejections set forth by the Examiner in the January 5, 2006 Office Action. Reconsideration of the application, as amended, is respectfully requested.

I. SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT & NOTICE OF COPENDING APPLICATIONS

Applicant hereby submits a Supplemental Information Disclosure Statement & Notice of Copending Application. The Supplemental Information Disclosure Statement cites references from the copending application. While the Applicant does not believe that these references will affect the patentability of the pending claims, Applicant respectfully requests the Examiner to consider the pending claims in connection with these references in order to make them of record.

II. THE SPECIFICATION

The Examiner asserts that element 210 in Figure 2B (drawing sheet 3) and Figure 3B (drawing sheet 5) shows a low pass filter. Therefore, the Examiner objected to the disclosure because Paragraph 47 of the specification refers to an integrator circuit 210. Applicant respectfully submits that the element 210 comprising a resistor 218 and a capacitor 220 can be properly interpret as an integrator circuit or a low pass filter. Indeed, an integrator circuit is one type of low pass filter. Thus, Applicant submits that the drawings are consistent with the specification and no correction is required.

III. OBJECTIONS TO CLAIMS 1 AND 11

The Examiner objected to Claims 1 and 11 because both claims are punctuated with two periods. In response, Applicant has amended the claims to remove the extra periods.

IV. REJECTION OF CLAIMS 1-10 UNDER 35 U.S.C. § 103(a)

The Examiner rejected Claims 1-10 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,157,182 issued to Tanaka, et al. ("the Tanaka patent") in view of U.S. Patent No. 6,229,293 issued to Farrenkopf ("the Farrenkopf patent") and U.S. Patent No. 6,204,650 issued to Shimamori ("the Shimamori patent"). In view of the above claim amendments and the following discussion, Applicant respectfully traverses this rejection.

A. Claim 1

Focusing in particular on Claim 1 and the embodiment shown in Figures 2A and 2B, a power converter comprises a switching transistor 106 and a pulse frequency modulator 108 configured to control the switching transistor 106. The pulse frequency modulator 108 is enabled during a burst period in which an output of the power converter (V-FB) is less than a predetermined level (V-REF). A peak current detector 200 senses current through the switching transistor 106 and outputs a peak current pulse to the pulse frequency modulator 108 to turn off the switching transistor 106 when the sensed current (I-SENSE) exceeds a peak reference level (I-REF). The peak reference level (I-REF) is substantially constant (HYST-LEVEL) during a hysteretic mode and is variable (CSM-LEVEL) during a continuous switching mode. A load sensor 214 monitors the output of the peak current detector 200 to change operating modes for the power converter. The power converter changes from the hysteretic mode to the continuous switching mode when the number of peak current pulses in the burst period exceeds a predetermined number.

The Tanaka patent appears to teach a dual-mode converter that uses two sets of control circuits to drive a switch. Referring to Fig. 9 of the Tanaka patent, a switch 21 is coupled to an input voltage (Vin) and selectively turns on/off to generate an output voltage (Vout) connected to a load. For light load currents, the switch 21 is controlled by a light load mode controlling circuit comprising comparators 25, 26 that sense a charging current (I_L) and a comparator 22 that senses the output voltage (Vout). For heavy load currents, the switch 21 is controlled by a PWM controlling circuit 45 that senses the output voltage (Vout). Control signals at respective outputs of the light load mode controlling circuit and the PWM controlling circuit 45 are provided to selectors 43, 44. A mode switching controlling circuit 49 determines whether the converter is

operating under light load currents or heavy load currents and controls the selectors 43, 44 to pass the appropriate control signals to drive the switch 21.

The Examiner asserts that Claim 1 of the present invention is taught by replacing the PWM controlling circuit 45 of the Tanaka patent with a PFM controller from the Shimamori patent and adapting the PFM controller for boost converter operation as discussed in the Farrenkopf patent. The Applicant respectfully disagrees with the Examiner's assertion.

First, there is no motivation to replace the PWM controlling circuit 45 of the Tanaka patent with a PFM controller. The Tanaka patent discloses using the light load mode controlling circuit and the PWM controlling circuit 45 to operate a converter in two modes to overcome deficiencies of a PFM system described in its background section. Thus, the Tanaka patent teaches away from replacing the PWM controlling circuit 45 with a PFM controller.

Second, the combination suggested by the Examiner does not teach Claim 1. Assuming that the PWM controlling circuit 45 is replaced with a PFM controller, the combination teaches a modified dual-mode converter that selects between the light load mode controlling circuit and the PFM controller to drive the switch 21 under different load current conditions. That is, the light load mode controlling circuit is used to control the switch 21 during light load currents while the PFM controller is used to control the switch 21 during heavy load currents. The combination does not teach a power converter with a pulse frequency modulator controlled by a peak current detector that uses a substantially constant peak reference level during a hysteretic mode and a variable peak reference level during a continuous switching mode.

Because the references cited by the Examiner do not disclose, teach or suggest a peak current detector that uses a substantially constant peak reference level during a hysteretic mode and a variable peak reference level during a continuous switching mode to generate a peak current pulse to a pulse frequency modulator, Applicant asserts that Claim 1 is not obvious in view of the Tanaka patent, the Farrenkopf patent and the Shimamori patent. Applicant therefore respectfully submits that Claim 1 is patentably distinguished over the cited reference and Applicant respectfully requests allowance of Claim 1.

B. Claims 2, 4 and 5

Claims 2, 4 and 5, which depend from Claim 1, are believed to be patentable for the same reasons articulated above with respect to Claim 1, and because of the additional features recited therein. Accordingly, Applicant respectfully requests allowance of Claims 2, 4 and 5.

C. Claim 6

Claim 6 is directed to a method to convert operating modes in a switching regulator. The method comprises the step of turning on a pulse frequency modulator for a burst period when an output of the switching regulator is less than a first level. One or more switching cycles for a switch occur in the burst period. An output from the pulse frequency modulator turns on the switch in each switching cycle until the switch conducts a peak current followed by a switch off-time of a predetermined duration. The pulse frequency modulator uses a substantially constant threshold to detect the peak current during a hysteretic mode and a variable threshold to detect the peak current during a continuous mode. The switching regulator converts from the hysteretic mode to the continuous mode when the number of switching cycles in a burst period exceeds a predetermined value.

The references cited by the Examiner do not disclose, teach or suggest a pulse frequency modulator that uses a substantially constant threshold to detect a peak current of a switch during a hysteretic mode and a variable threshold to detect the peak current of the switch during a continuous mode. Applicant therefore respectfully submits that Claim 6 is patentably distinguished over the cited references and Applicant respectfully requests allowance of Claim 6.

D. Claims 7, 9 and 10

Claims 7, 9 and 10, which depend from Claim 6, are believed to be patentable for the same reasons articulated above with respect to Claim 6, and because of the additional features recited therein. Accordingly, Applicant respectfully requests allowance of Claims 7, 9 and 10.

V. REJECTION OF CLAIMS 11 AND 12 UNDER 35 U.S.C. § 103(a)

The Examiner rejected Claims 11 and 12 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,433,525 issued to Muratov, et al. ("the Muratov patent") in view of the

Shimamori patent. In view of the above claim amendments and the following discussion, Applicant respectfully traverses this rejection.

A. Claim 11

Claim 11 is directed to a switching regulator using a dual-mode pulse frequency modulation technique. The switching regulator comprises means for sensing a transition from relatively light load current to relatively heavy load current by monitoring switching cycles of a switch. The switching regulator also comprises means for operating in a hysteretic mode during relatively light load current with a pulse frequency modulator using a first threshold to monitor current conducted by the switch during the hysteretic mode, and the switch conducts a substantially fixed peak current during the hysteretic mode. The switching regulator further comprises means for operating in a continuous switching mode with the pulse frequency modulator using a second threshold to monitor current conducted by the switch during the continuous switching mode, and the switch conducts a variable peak current during the continuous switching mode.

The Muratov patent appears to teach a DC-DC converter that selects between a PWM controller and a hysteretic controller to drive switches. Referring to Figure 4 of the Muratov patent, a dual mode converter 100 includes a mode control switch 50 that selects between outputs from a PWM controller and a hysteretic controller to a gate logic circuit for controlling switches. The hysteretic controller is used for light load currents while the PWM controller is used for heavy load currents.

The Examiner asserts that Claim 11 is taught by replacing the PWM controller in the Muratov patent with a PFM controller disclosed in the Shimamori patent. The Applicant respectfully disagrees with the Examiner's assertion. The combination suggested by the Examiner teaches using a hysteretic controller for light load currents and a separate PFM controller for heavy load currents.

Because the references cited by the Examiner do not disclose, teach or suggest a switching regulator with a pulse frequency modulator that uses different thresholds for different modes to monitor current conducted by a switch, Applicant asserts that Claim 11 is not obvious in view of the Muratov patent and the Shimamori patent. Applicant therefore respectfully

submits that Claim 11 is patentably distinguished over the cited references and Applicant respectfully requests allowance of Claim 11.

B. Claim 12

Claim 12, which depends from Claim 11, is believed to be patentable for the same reasons articulated above with respect to Claim 11, and because of the additional features recited therein. Accordingly, Applicant respectfully requests allowance of Claim 12.

VI. CONCLUSION

In view of the foregoing, the present application is believed to be in condition for allowance, and such allowance is respectfully requested. If further issues remain to be resolved, the Examiner is cordially invited to contact the undersigned such that any remaining issues may be promptly resolved. Also, please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1410.

Respectfully submitted,

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